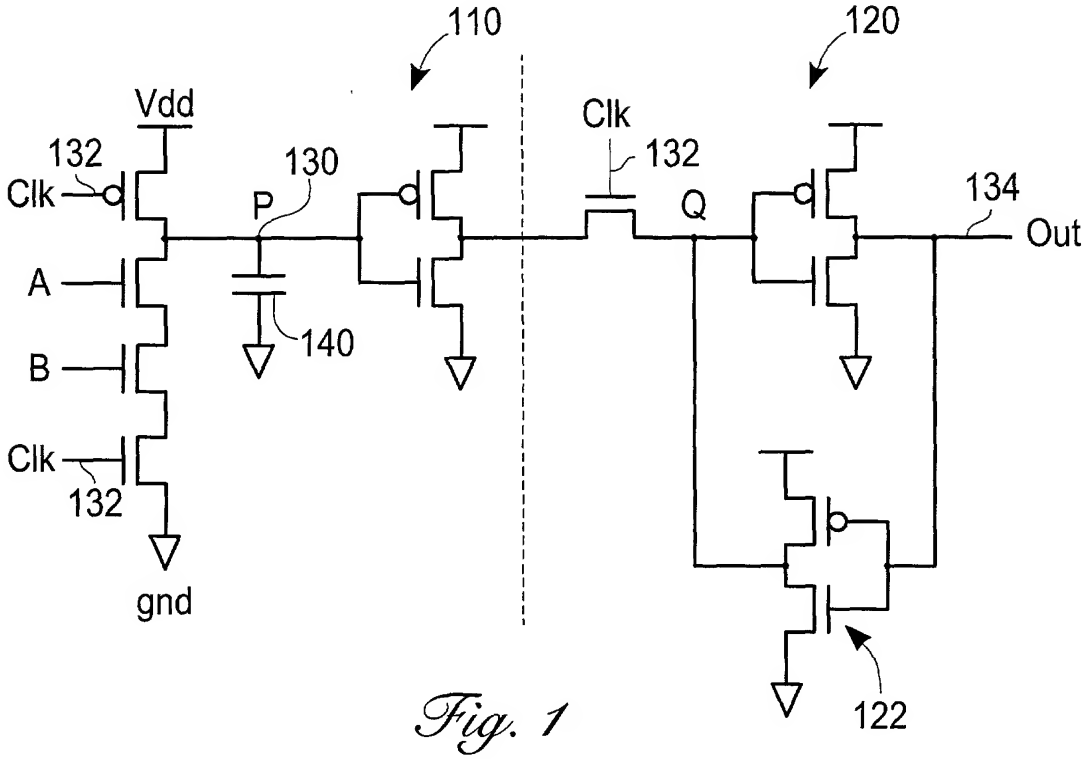

110
120
Vdd
Clk
132
130
Clk
132
P
Q
134
Out
A
B
140
Clk
132
gnd
122

Fig. 1

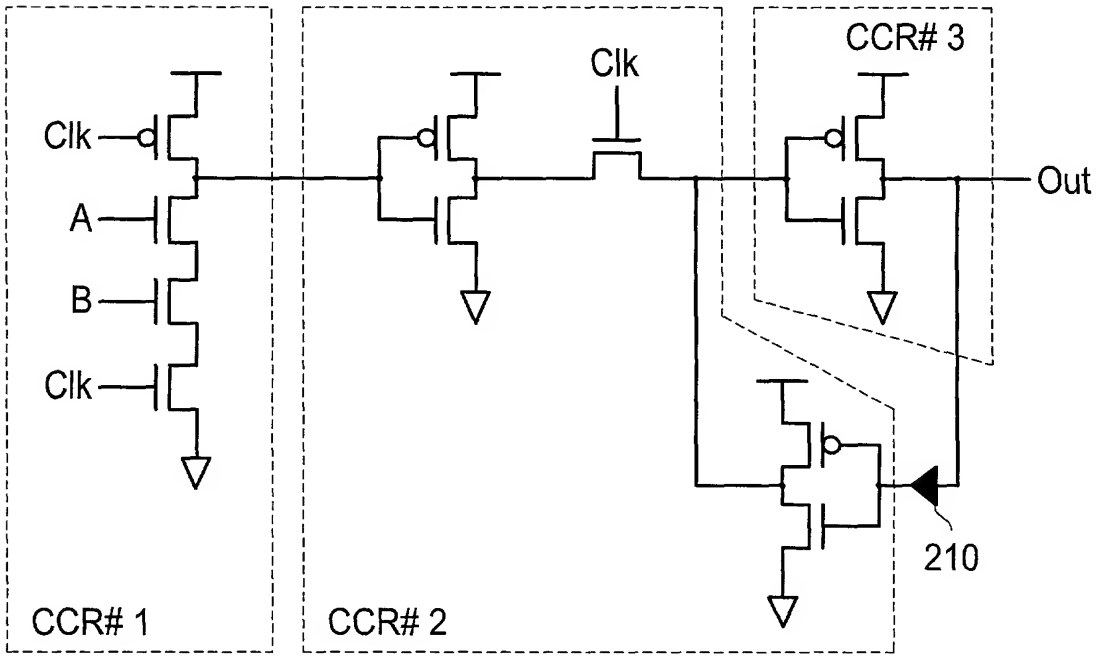
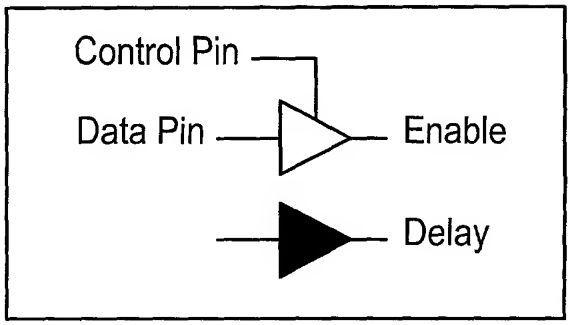

CCR# 3
Clk
Clk
Out
A
B
Clk
210
CCR# 1
CCR# 2

Fig. 2


Control Pin
Data Pin
Enable
Delay

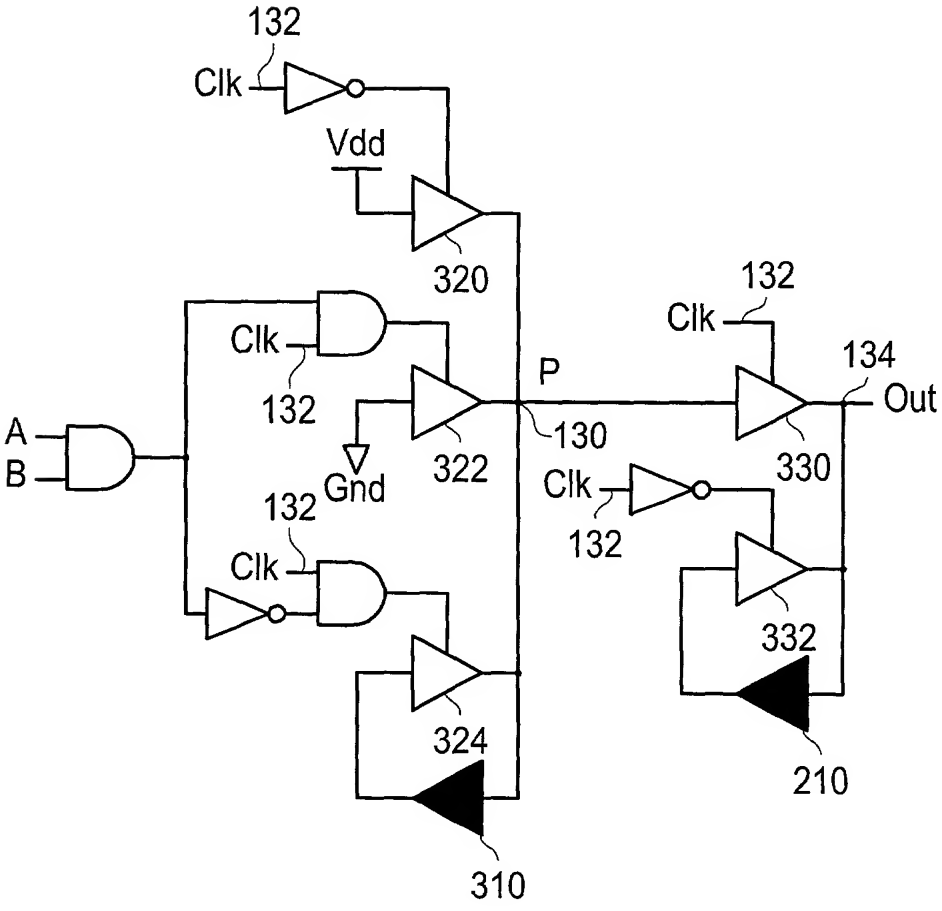

132
Clk
Vdd
320
Clk
132
A
B
Gnd
322
P
130
132
Clk
330
134
Out
Clk
132
132
Clk
332
324
210
310

Fig. 3

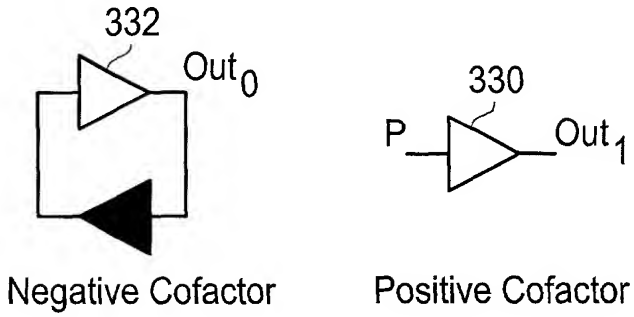

332
Out0
330
P
Out1
Negative Cofactor
Positive Cofactor

Fig. 4

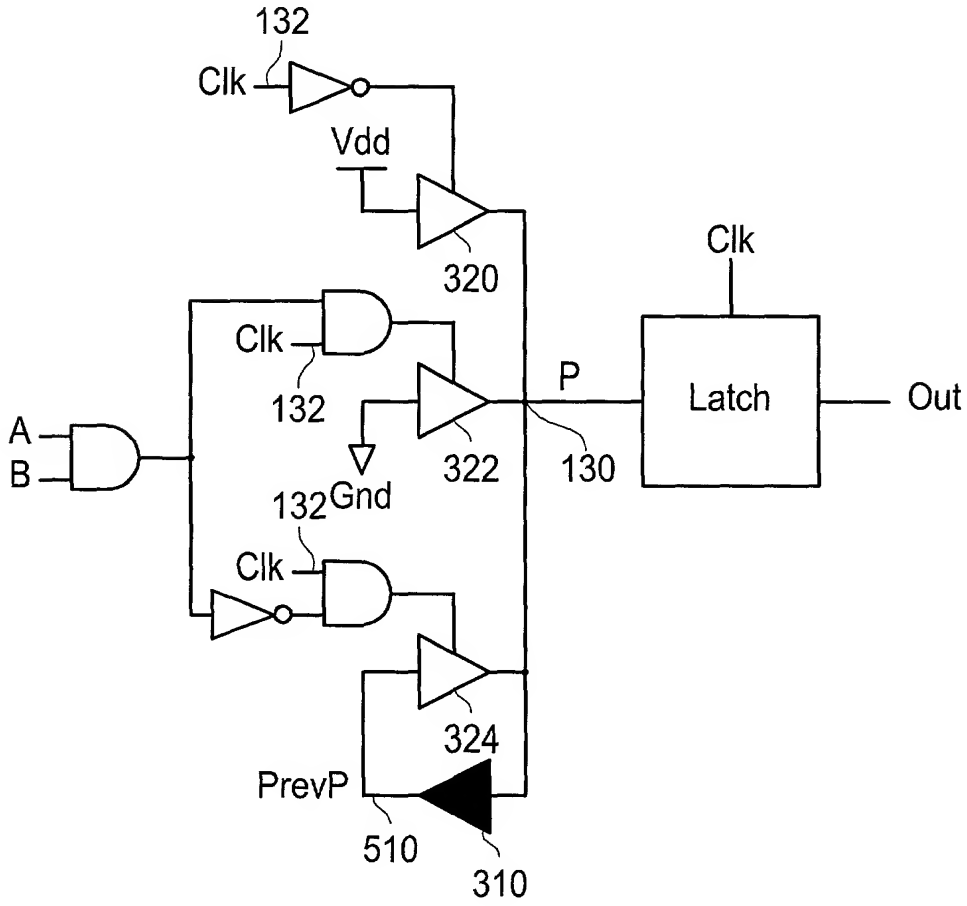

132
Clk
Vdd
320
Clk
Clk
132
P
Latch
Out
A
B
322
130
132
Gnd
Clk
324
PrevP
510
310

Fig. 5

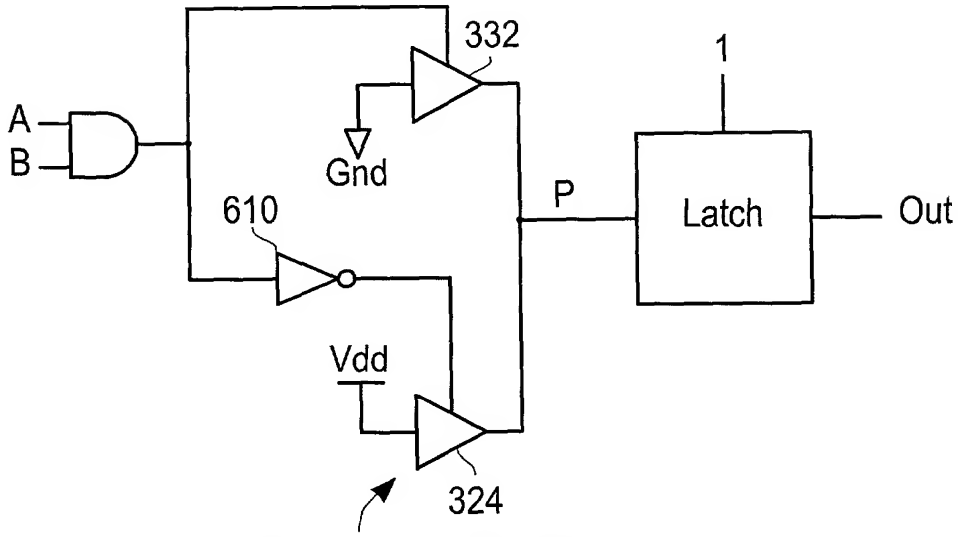


Fig. 6

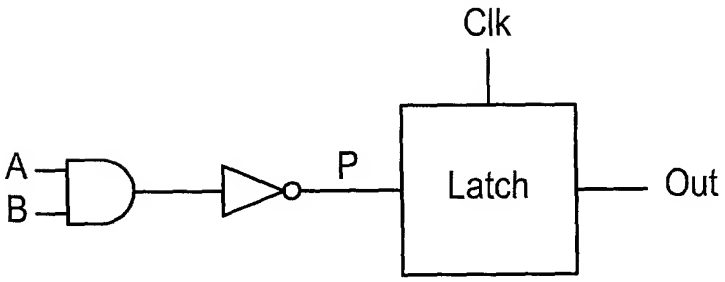


Fig. 7

Portal Ex. 2054 Page 4 of 54

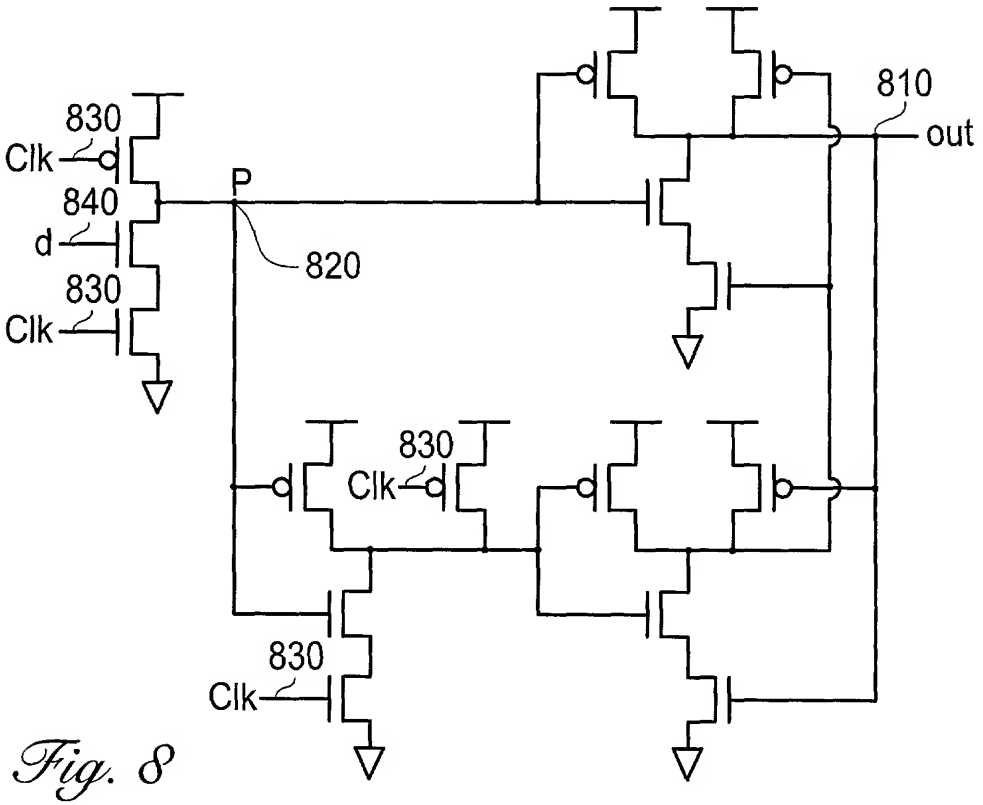


Fig. 8

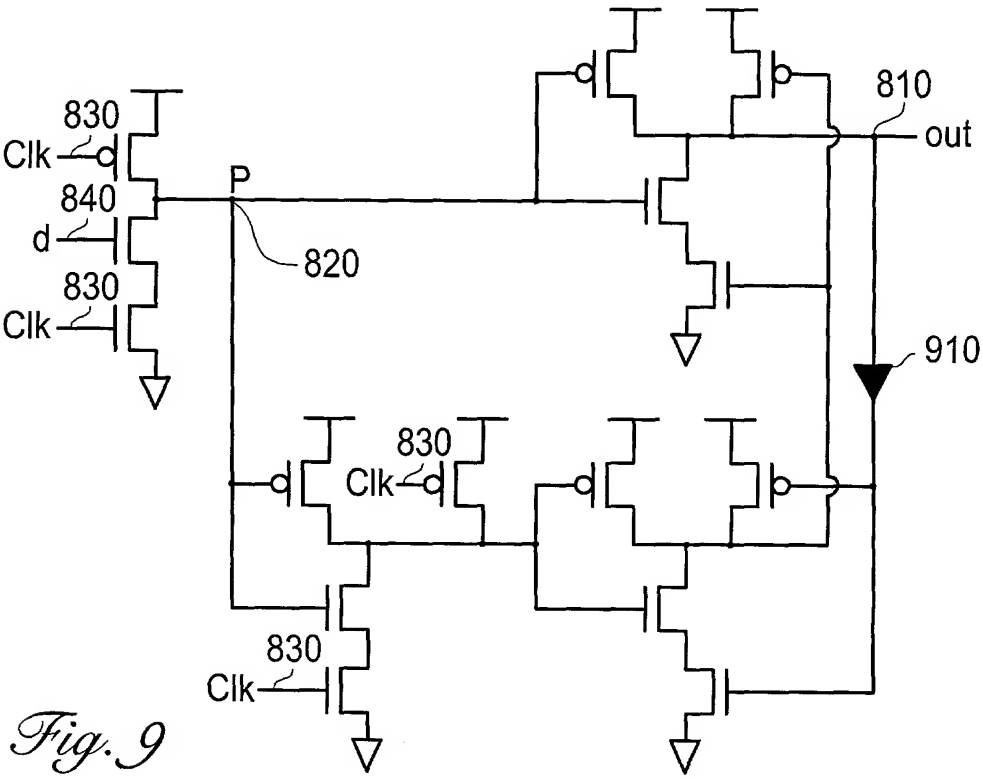


Fig. 9

Attorney Docket No. 15448-0506

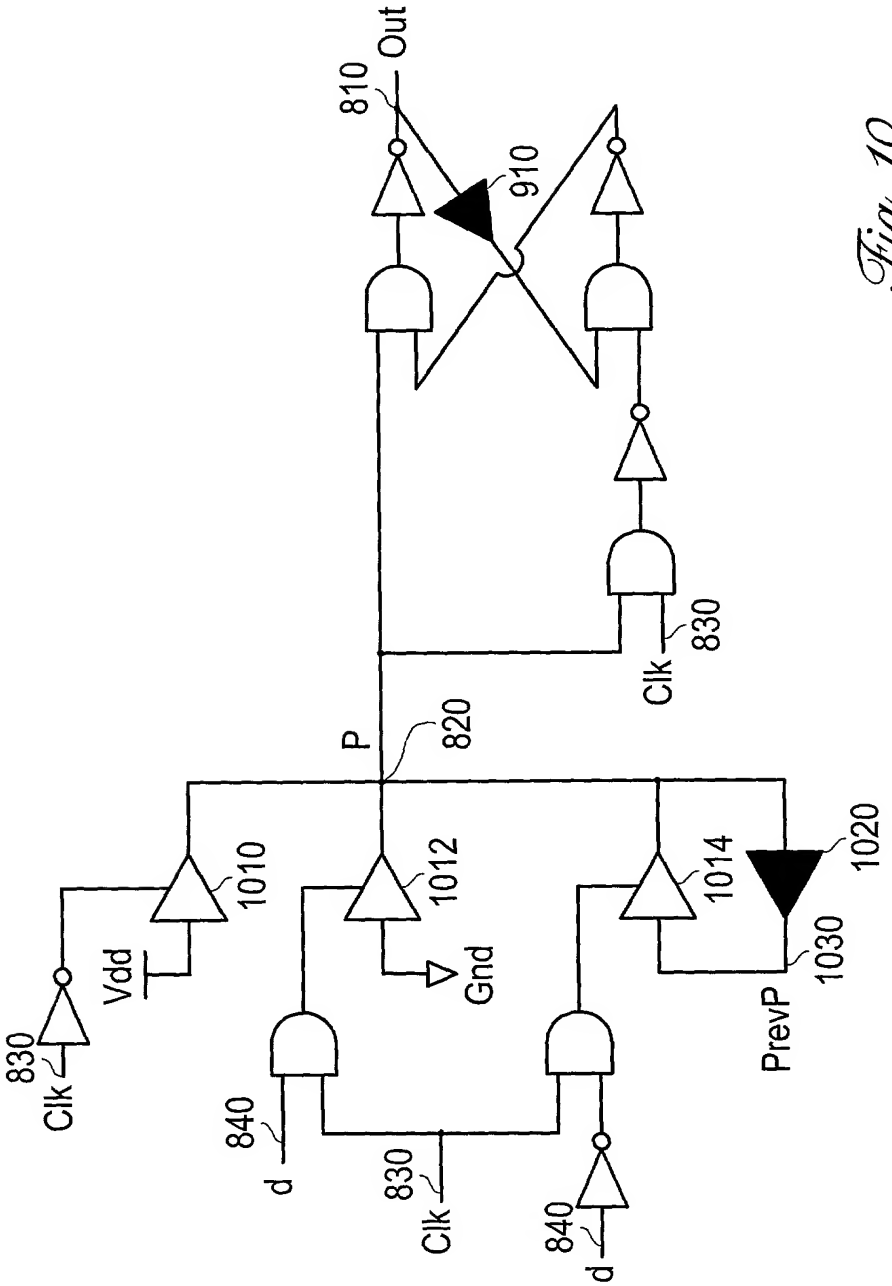

Out
810
910
830
Clk
P
820
1010
1012
1014
1020
1030
Vdd
Gnd
PrevP
830
Clk
840
d
830
Clk
840
d

Fig. 10

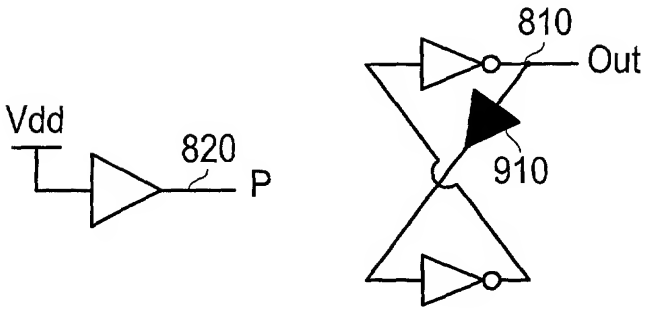


Fig. 11

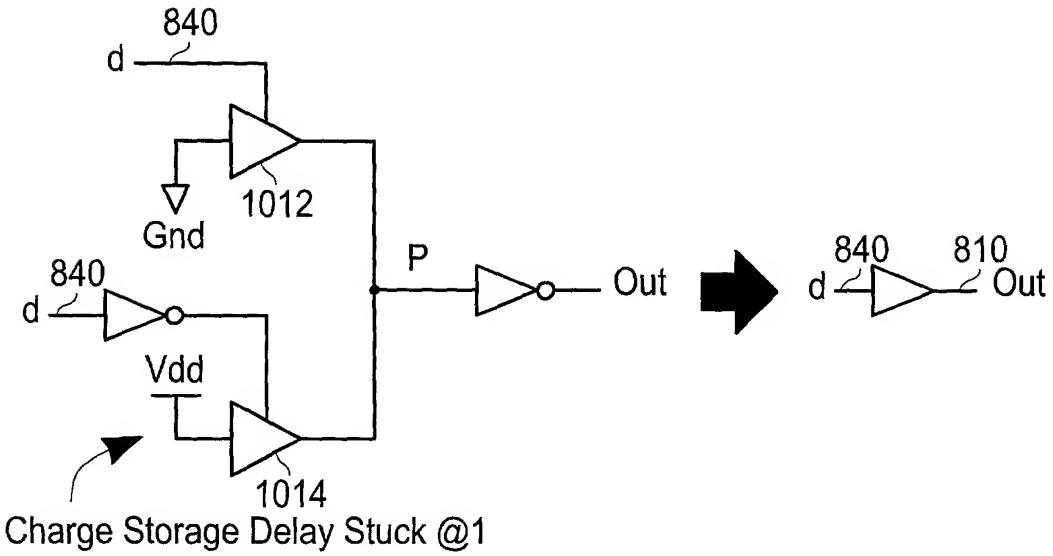


Fig. 12

Patent-5,974,568

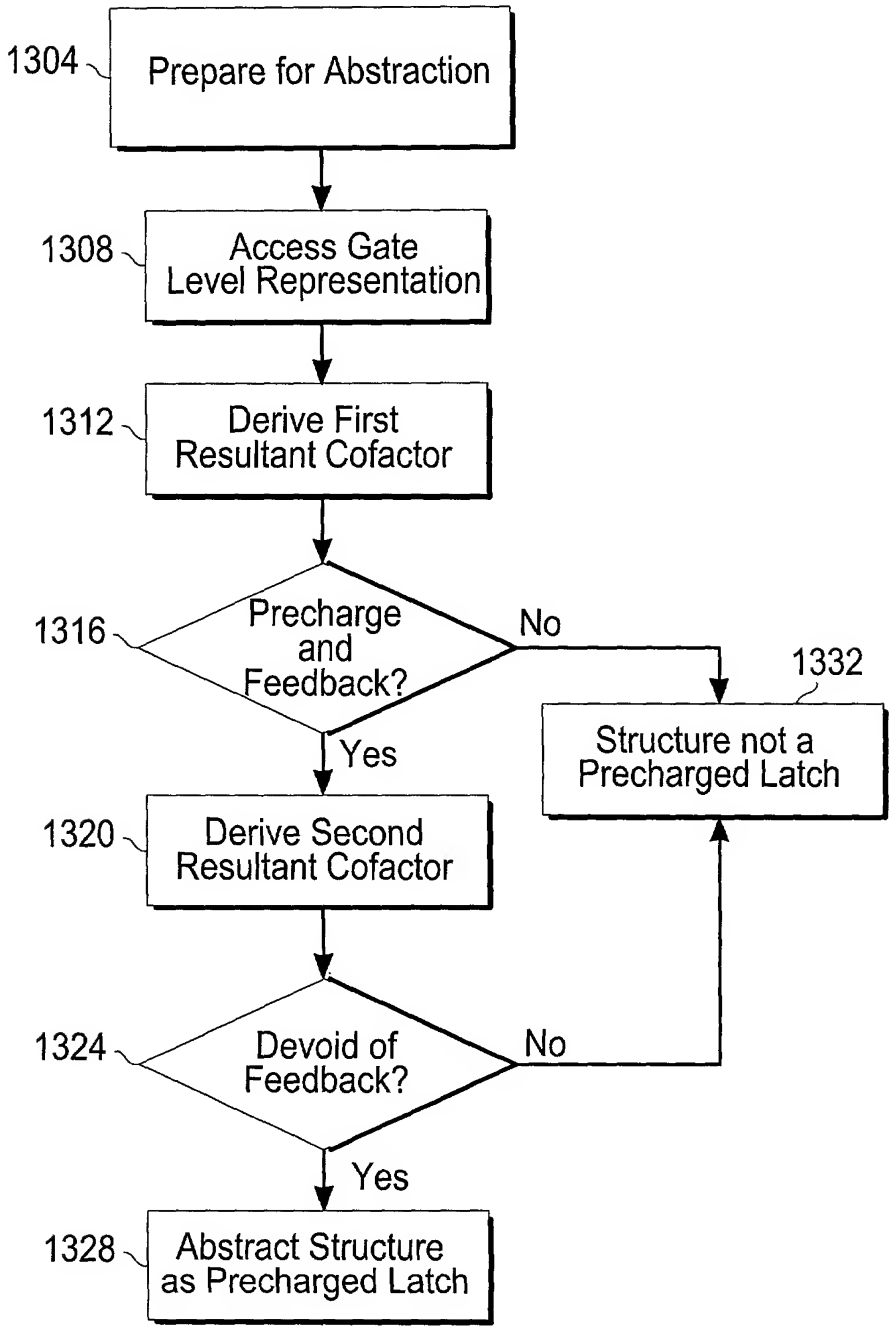


Fig. 13

Portal Snapshot

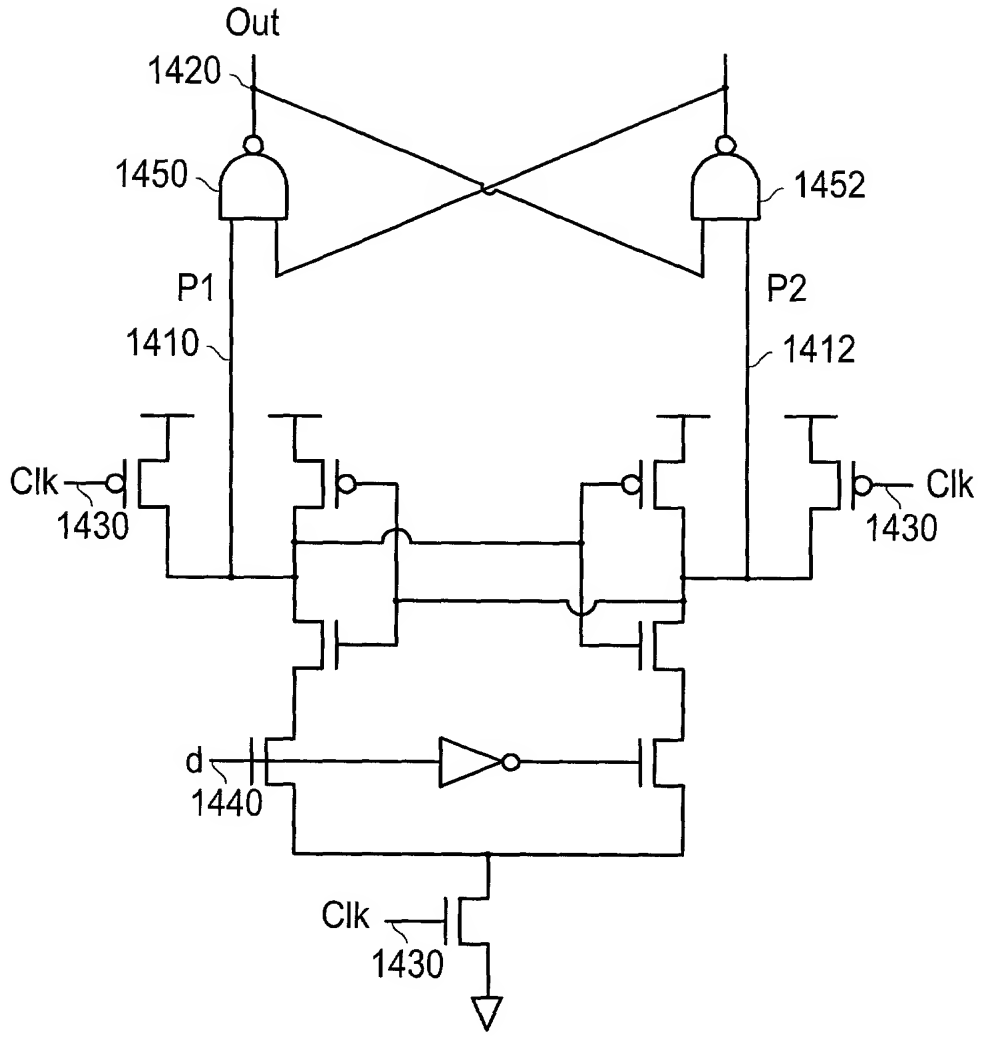

Out
1420
1450
1452
P1
P2
1410
1412
Clk
1430
Clk
1430
d
1440
Clk
1430

Fig. 14

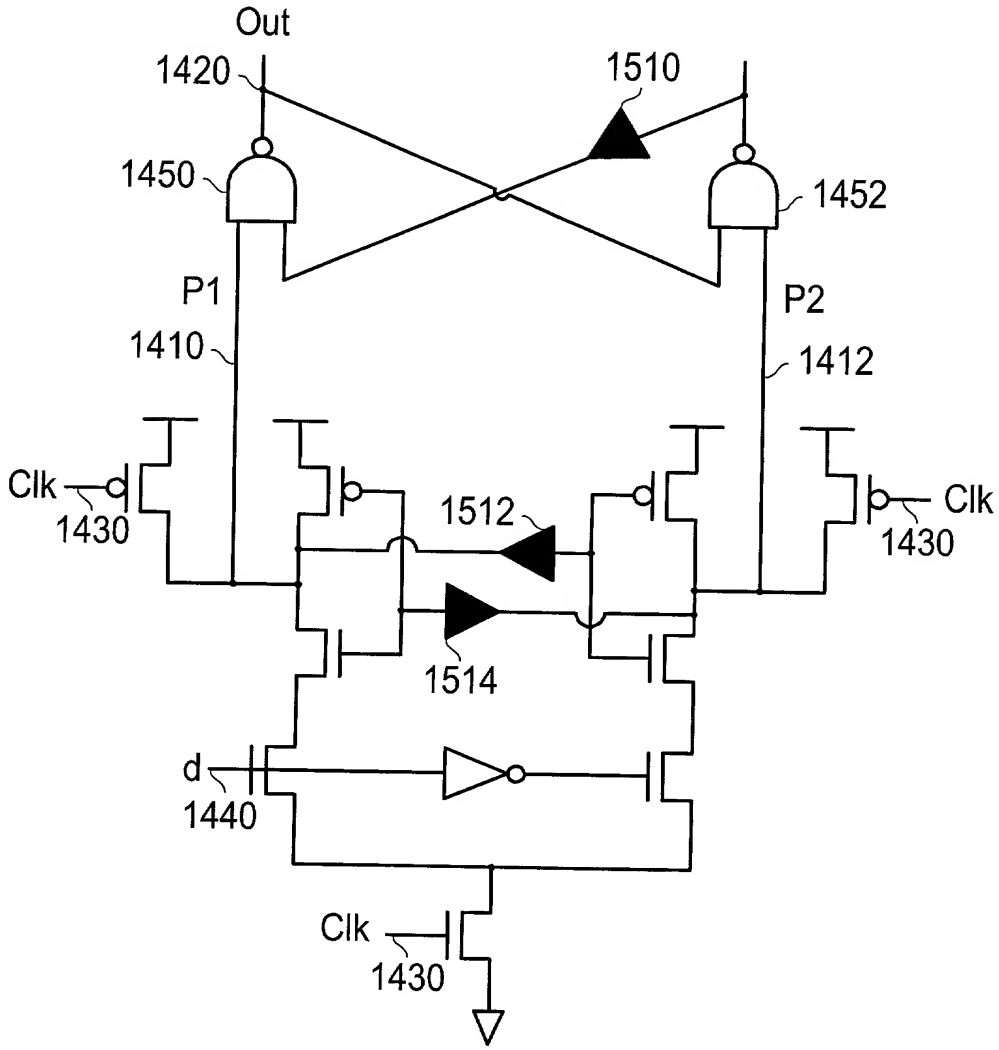

Out
1420
1510
1450
1452
P1
P2
1410
1412
Clk
1430
1512
Clk
1430
1514
d
1440
Clk
1430

Fig. 15

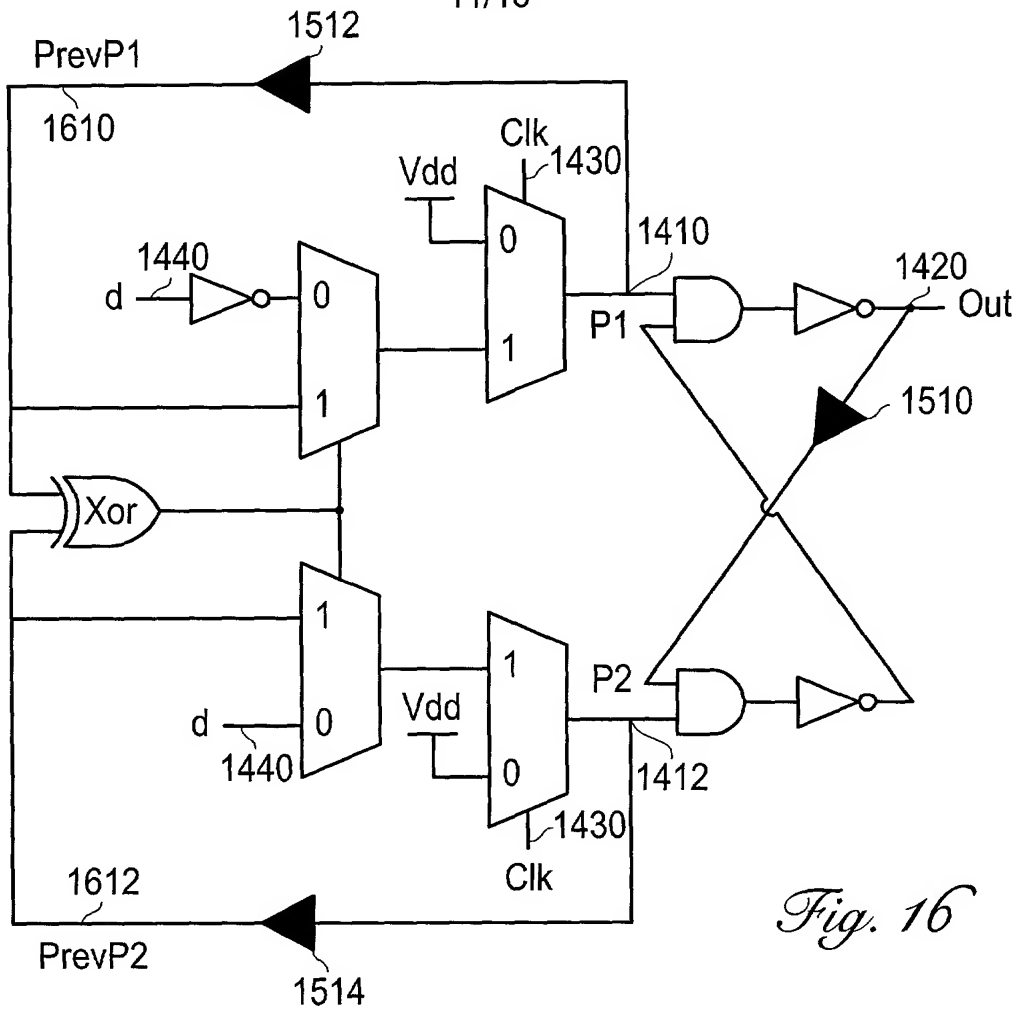


Fig. 16

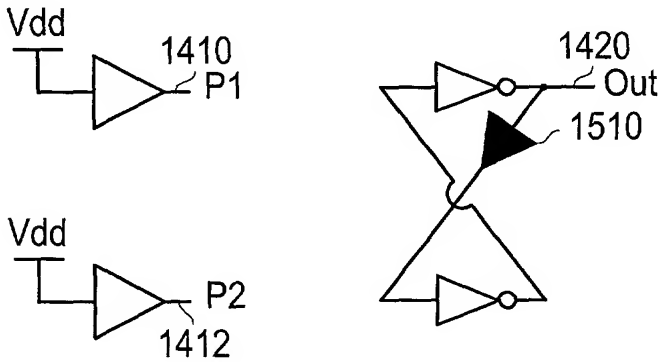


Fig. 17

Docket No.: 15448-0506

15448-0506

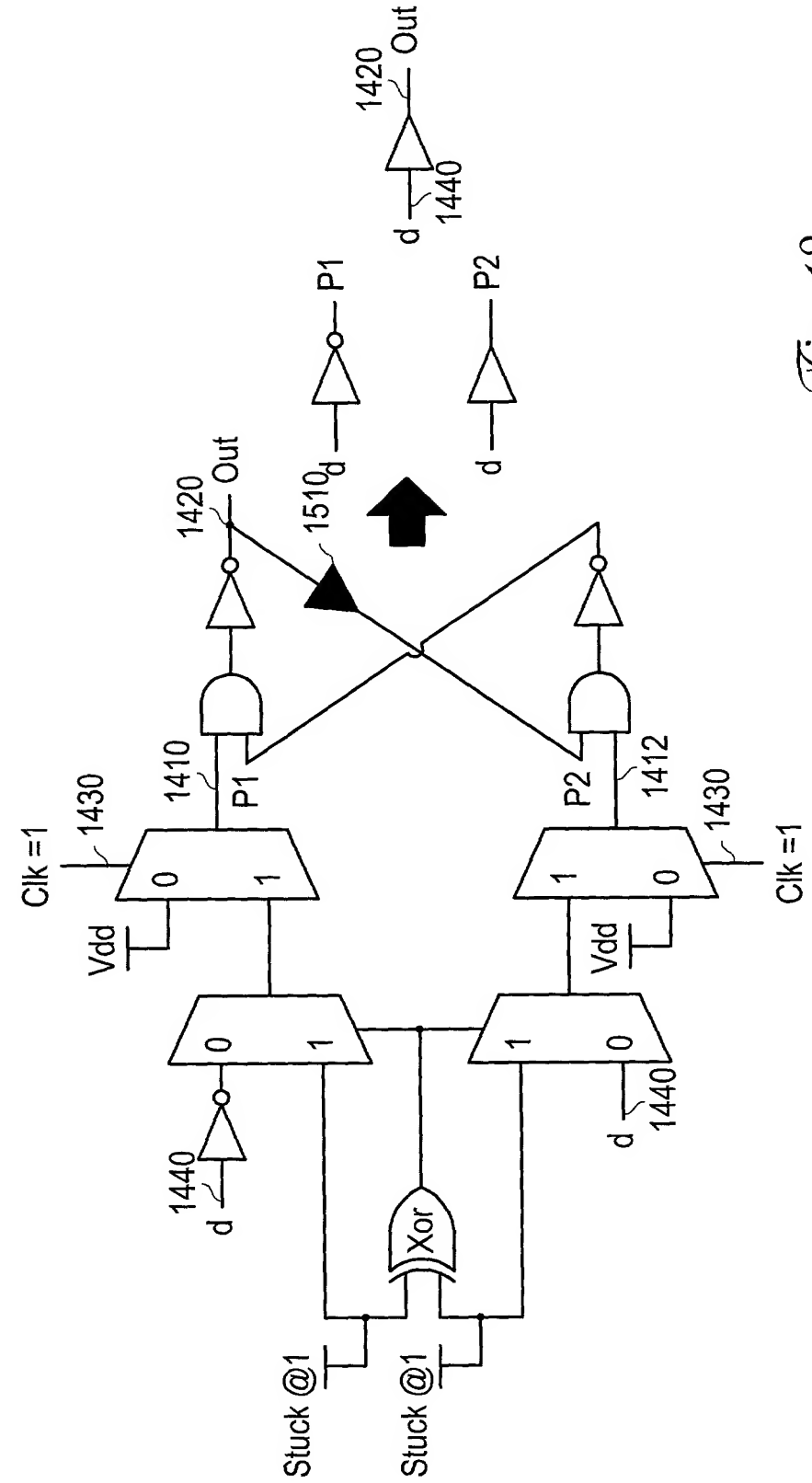


Fig. 18

Confidential

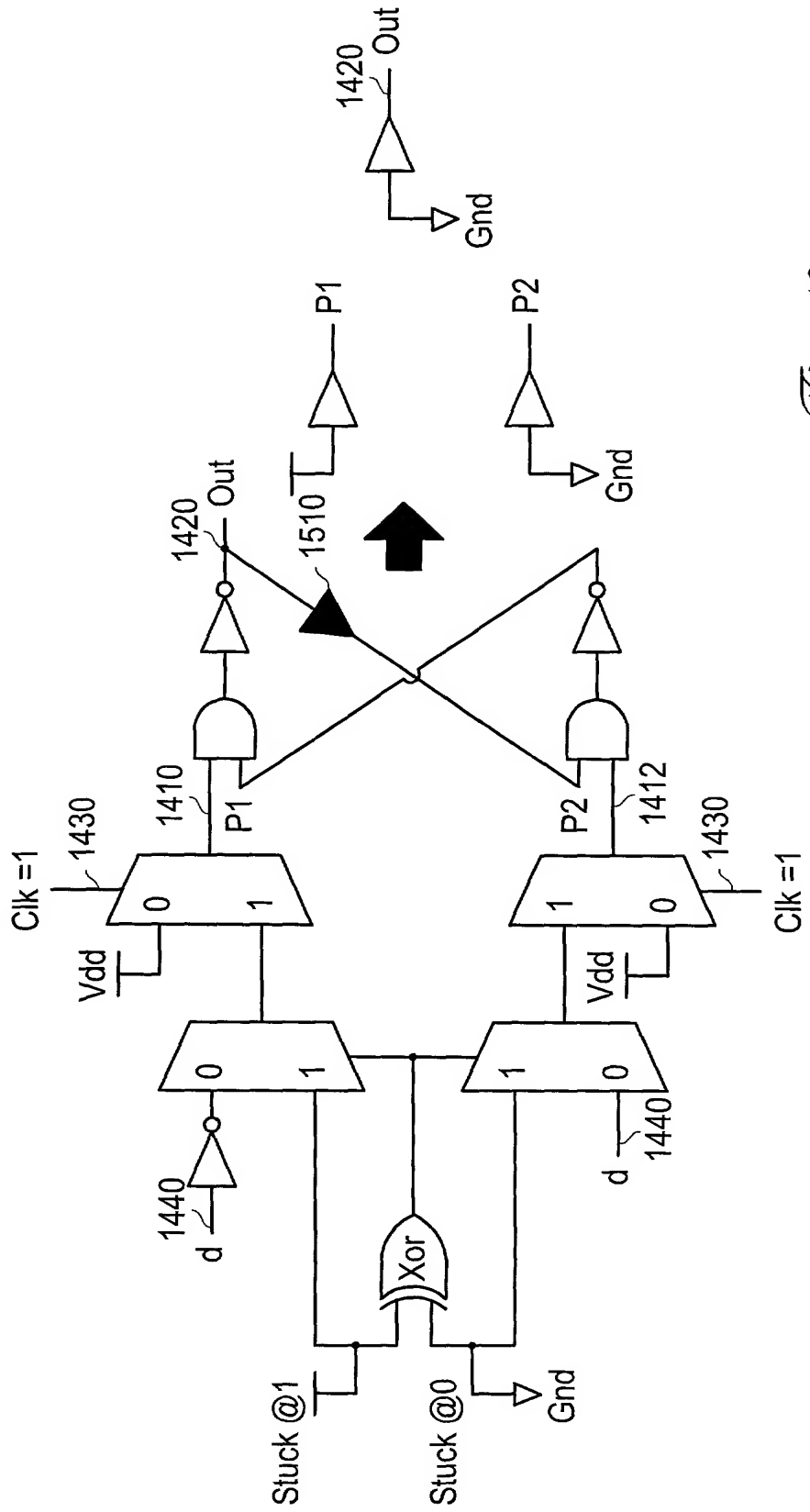


Fig. 19

Total Patent

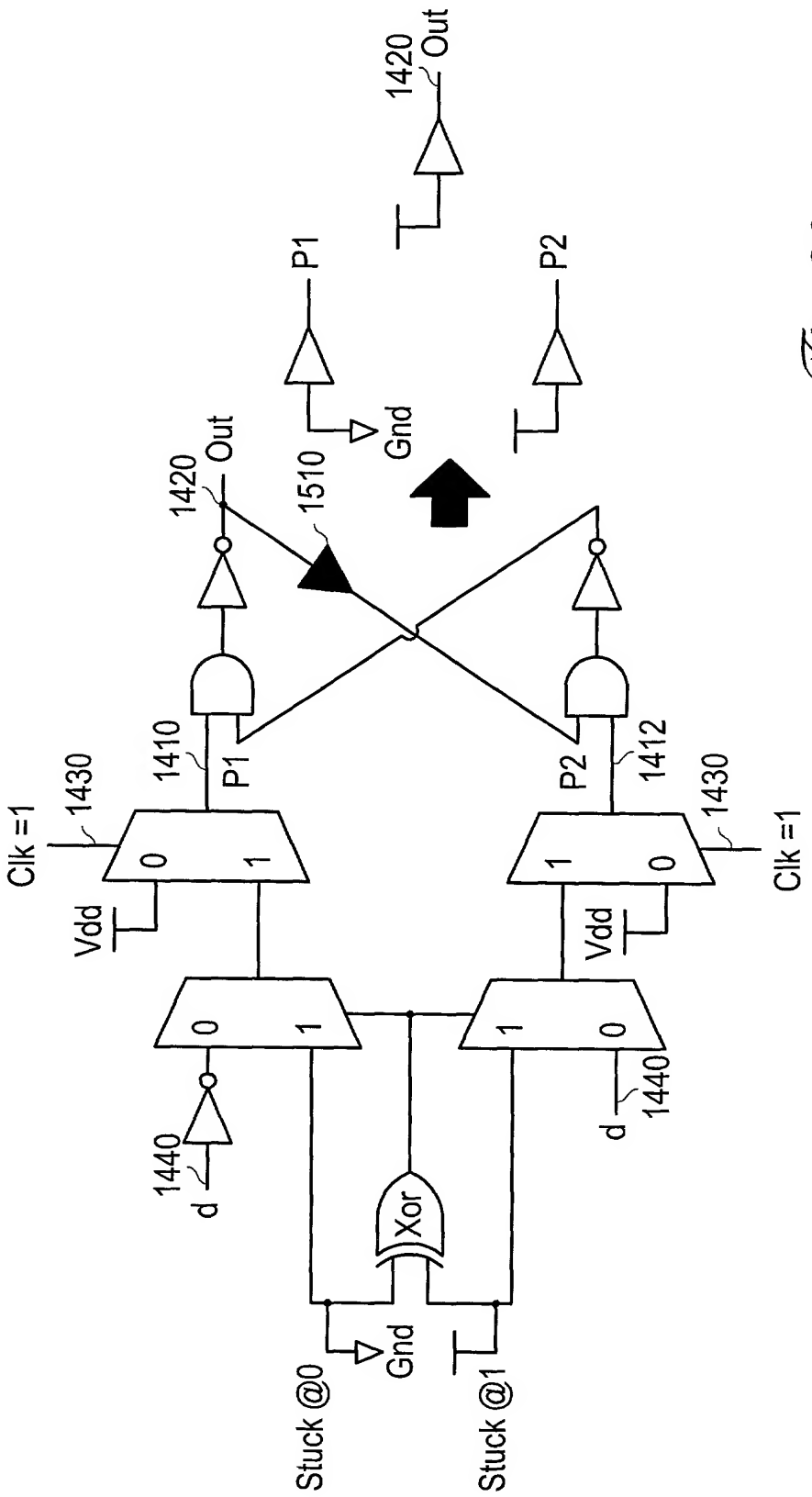


Fig. 20

FORMAT SAMPLE

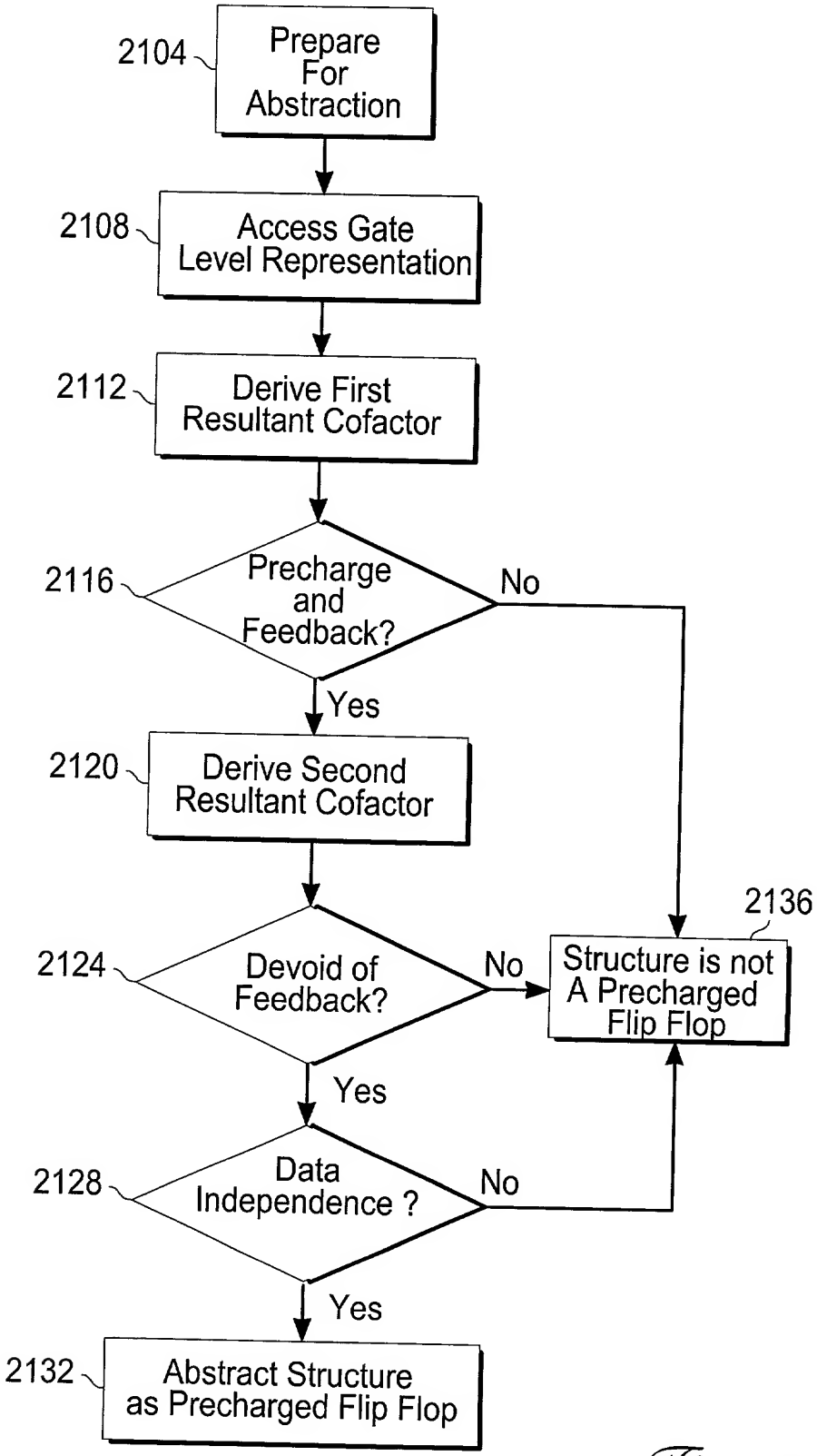

2104
Prepare For Abstraction
2108
Access Gate Level Representation
2112
Derive First Resultant Cofactor
2116
Precharge and Feedback?
No
Yes
2120
Derive Second Resultant Cofactor
2124
Devoid of Feedback?
No
2136
Structure is not A Precharged Flip Flop
Yes
2128
Data Independence ?
No
Yes
2132
Abstract Structure as Precharged Flip Flop

Fig. 21

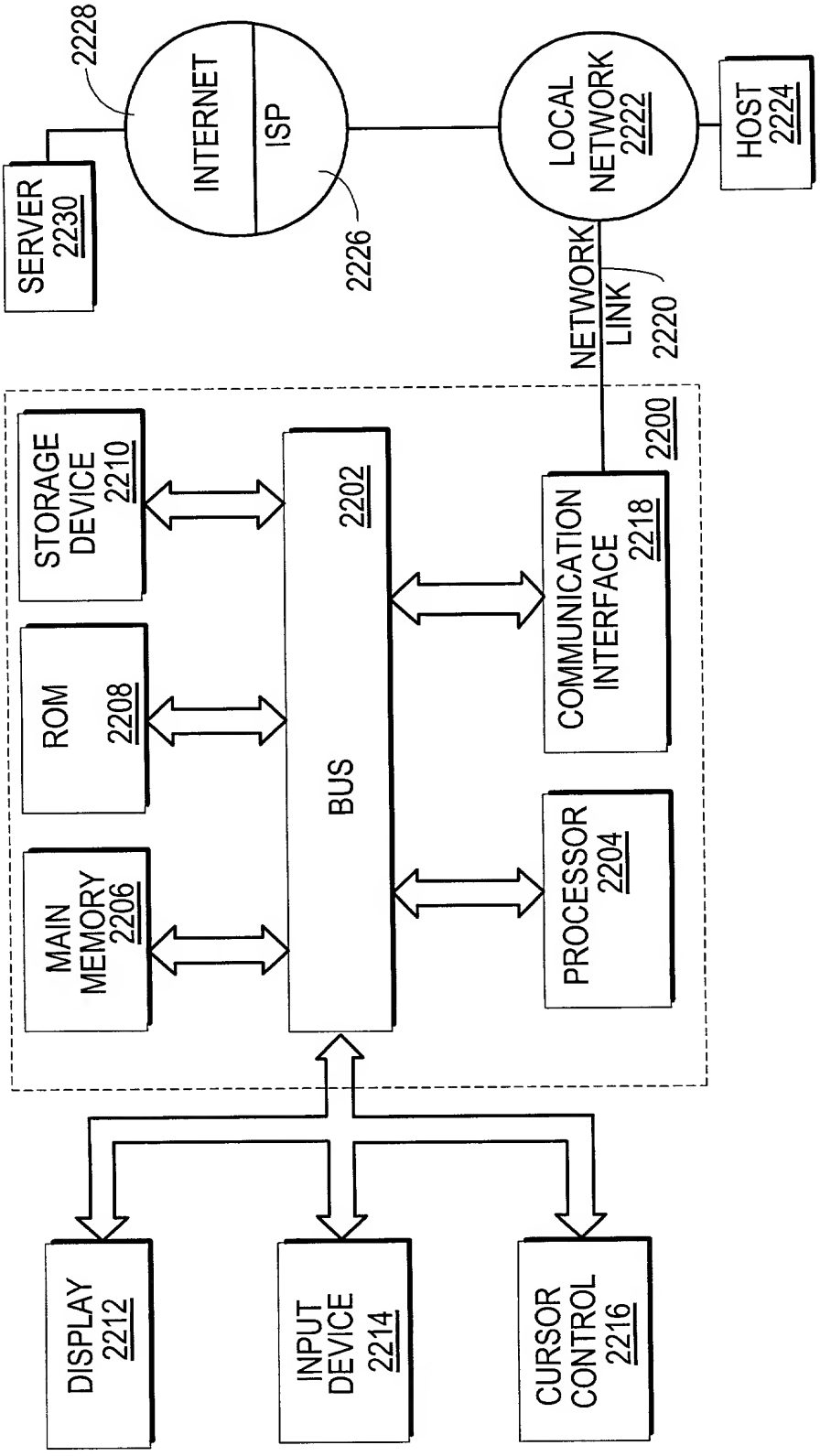

2228
INTERNET
ISP
2226
SERVER 2230
LOCAL NETWORK 2222
HOST 2224
NETWORK LINK 2220
2200
STORAGE DEVICE 2210
ROM 2208
MAIN MEMORY 2206
BUS 2202
COMMUNICATION INTERFACE 2218
PROCESSOR 2204
DISPLAY 2212
INPUT DEVICE 2214
CURSOR CONTROL 2216

Fig. 22